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controlling a device via interface read "write"

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[Variable capacity data buffer system](#)

CA Heath - US Patent 4,258,418, 1981 - Google Patents

 ... line 86 to switch 30 for **controlling** the application ... storage capacity of data buffer storage **device** 10 that ... through channel hv terface 62 and **via** signal line ...

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[Data processing system having automatic configuration](#)

BV Shah, JA Maskevitch - US Patent 4,589,063, 1986 - Google Patents

 ... controllers, analog-to-digital interfaces, computer network **interface** equipment can ... link shown ena -bles the system to **control** the I/O **device via** the driver ...

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[Method and apparatus for dynamically **controlling read/write** operations in a peripheral subsystem](#)

S Patel - US Patent 3,950,735, 1976 - freepatentsonline.com

 ... microprocessor 126 then polls the selected peripheral **device via** the DLI **control** 134 to ... generally different for different magnetic tape **device** models and ...

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[Interface adaptor emulating magnetic tape drive](#)

DA Birkner, MA Sankey - US Patent 4,727,512, 1988 - freepatentsonline.com

 ... fact that magnetic tape transport **device** manufactures, for ... multiplexer 40, micro sequencer 48, **control** store unit ... peripheral processing system 11 **via** the host ...

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[Multi-processor, multi-bus system with bus **interface** comprising FIFO register stocks for receiving ...](#)

RJ Ternes, CA Huey, RW Bruner - US Patent 4,935,894, 1990 - freepatentsonline.com

 ... is passed to **control** logic means 64 **via** line 70 ... required functions such as Integrated **Device** Technology Part ... Interrupt **control** means 62 sends **control** signals to ...

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[... for fibre channel transmission having **interface** logic, buffer memory, multiplexor/control **device**, ...](#)

CE Nogales, WG Sooy - US Patent 5,809,328, 1998 - freepatentsonline.com

 ... and from the peripheral storage subsystem **via** the buffer ... processor bus; and, a bus **control device** coupled between ... service requests of the **interface** logic, the ...

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[General purpose parallel port **interface**](#)

RJ Proesel - US Patent 5,390,321, 1995 - Google Patents

 ... signals from the **device** to the CPU 22. ... **control** block 50 **via** the upper four bits of the data lines ... The command decoder and main **control** block 50 ...

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[... data between an IEEE 1394 bus and a **device** to be controlled by a control signal transmitted **via** the ...](#)

HH Hake, T Heighway, HW Keesen - US Patent 6,247,083, 2001 - freepatentsonline.com

 ... available within LLI1 as internal **control** signal CTL_INT ... be transferred between PLI and LLI1 **via** an isolation ... are both assigned to the same application **device**. ...

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[Multiple port bus **interface** controller with slave bus](#)

KB DuLac - US Patent 4,935,868, 1990 - freepatentsonline.com

... of **control** lines, and to the data buffer **device via** a third ... as host processor 12
or IEEE 796 **device** 13. ... in the auto-incrementing mode under the **control** of any ...

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Communication control unit

JS Davis, KN Larson, FW Phalen - US Patent 4,075,691, 1978 - Google Patents

... The sequence of **control** signals on the Unibus is as follows: 50 ... 4) Slave **device**
(core memory ... Input data is transferred to the PCM **via** the input data multiplexer ...

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Key authors: [D Golub](#) - [B Shah](#) - [K Larson](#) - [M Farmwald](#) - [J Davis](#)

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